

WHAT IS CLAIMED IS:

1. A computer-implemented method for controlling metal line resistance (RS) uniformity in a semiconductor manufacturing process using integrated or in-line metrology, comprising the steps of:

(A) collecting first data representative of at least one measurement of a first thickness of at least one deposition layer, subsequent to a deposition process on at least one semiconductor product;

(B) collecting second data representative of a plurality of measurements characterizing a profile of at least one trench in the at least one deposition layer, subsequent to an etch process on the at least one semiconductor product;

(C) collecting third data representative of at least one measurement of a second thickness of the at least one deposition layer, and a thickness of a metal deposited in the at least one trench, on the at least one semiconductor product;

(D) determining an area of a cross section of metal in the at least one trench at the profile and comparing the resistance of the area to a target resistance; and

(E) determining a planarization process to adjust an amount of metal in the at least one trench to approximate the target resistance in the at least one semiconductor product.

2. The method of claim 1, further comprising utilizing the determined planarization process for at least one of: the at least one semiconductor product, another semiconductor product subsequent to the at least one semiconductor product, a lot of semiconductor products including the at least one semiconductor product, and a lot of semiconductor products including the other semiconductor product.

3. The method of claim 1, further comprising utilizing at least one of: the first data to adjust the deposition process, the second data to adjust a lithography process and/or the etch process, and the third data to adjust the planarization process.

4. The method of claim 1, further comprising determining a variation in resistance over a plurality of semiconductor products including the at least one semiconductor product.
5. The method of claim 1, wherein the at least one deposition layer includes a dielectric deposition layer, and wherein the deposition process is a chemical vapor deposition process.
6. The method of claim 1, wherein the plurality of measurements characterizing the profile include at least depth, top critical dimension, bottom critical dimension, and at least one critical dimension along a side wall of the at least one trench.
7. The method of claim 1, wherein the third data includes data representative of a dishing and/or erosion of the method in the at least one trench.
8. The method of claim 1, wherein the determined planarization process includes at least one of a removal rate, a polishing pressure, and chemical supplies to be used.
9. The method of claim 1, further comprising the step of measuring the actual resistance of metal in the at least one trench, and comprising the actual resistance to the target resistance.
10. A computer-implemented method for improving and controlling metal line resistance (RS) uniformity in a semiconductor manufacturing process using integrated or in-line metrology, comprising the steps of:
 - (A) collecting first data representative of at least one measurement of a first thickness of at least one dielectric deposition layer, subsequent to a chemical vapor deposition process on at least one semiconductor product;
 - (B) collecting second data representative of a plurality of measurements characterizing a profile of at least one trench in the at least one dielectric deposition layer, including at least depth, top critical dimension, bottom critical dimension, and at least one critical dimension along a side wall, of the at least one trench, subsequent to an etch process on the at least one semiconductor product;
 - (C) collecting third data representative of at least one measurement of a second thickness of the at least one dielectric deposition layer, a thickness of a metal deposited in the at

least one trench, and a dishing and/or erosion of the metal in the at least one trench, on the at least one semiconductor product;

(D) determining an area of a cross section of metal in the at least one trench at the profile, and comparing the resistance of the area to a target resistance;

(E) determining at least one of a removal rate, polishing pressure, and chemical supplies to use in the chemical mechanical planarization process, to leave an amount of metal in the at least one trench, approximating the target resistance in the at least one semiconductor product;

(F) utilizing the at least one of the determined removal rate, polishing pressure, and chemical supplies in the chemical mechanical planarization process for at least one of: the at least one semiconductor product, another semiconductor product subsequent to the at least one semiconductor product, a lot of semiconductor products including the at least one semiconductor product, and a lot of semiconductor products including the other semiconductor product;

(G) utilizing at least one of: the first data to adjust the CVD process, the second data to adjust the litho and etch process, and the third data to adjust the CMP process, for the other semiconductor product subsequent to the at least one semiconductor product; and

(H) determining a variation in resistance over the plurality of semiconductor products including the at least one semiconductor product.

11. A computer-assisted system for controlling metal line resistance (RS) uniformity, in a semiconductor manufacturing process using integrated or in-line metrology components, comprising:

(A) at least one first component, to collect first data representative of at least one measurement of a first thickness of at least one deposition layer, subsequent to a deposition process on at least one semiconductor product;

(B) at least one second component, to collect second data representative of a plurality of measurements characterizing a profile of at least one trench in the at least one deposition layer, subsequent to an etch process on the at least one semiconductor product;

(C) at least one third component, to collect third data representative of at least one measurement of a second thickness of the at least one deposition layer, and a thickness of a metal deposited in the at least one trench, on the at least one semiconductor product; and

(D) at least one controller, communicating with the at least one first component, the at least one second component, and the at least one third component, to determine an area of a cross section of metal in the at least one trench at the profile, and to compare the resistance of the area to a target resistance; and to determine a planarization process, so as to leave an amount of metal in the at least one trench, approximating the target resistance in the at least one semiconductor product.

12. The system of claim 11, wherein the at least one controller utilizes the determined planarization process for at least one of: the at least one semiconductor product, another semiconductor product subsequent to the at least one semiconductor product, a lot of semiconductor products including the at least one semiconductor product, and a lot of semiconductor products including the other semiconductor product.

13. The system of claim 11, wherein the deposition process, responsive to the first data, adjusts the deposition process; a lithography process and/or the etch process, responsive to the the second data, adjusts the lithography process and/or the etch process; and the planarization process, responsive to the third data, adjusts the planarization process.

14. The system of claim 11, wherein the at least one controller determines a variation in resistance over a plurality of semiconductor products including the at least one semiconductor product.

15. The system of claim 11, wherein the at least one deposition layer includes a dielectric deposition layer, and wherein the deposition process is a chemical vapor deposition process.

16. The system of claim 11, wherein the plurality of measurements characterizing the profile include at least depth, top critical dimension, bottom critical dimension, and at least one critical dimension along a side wall of the at least one trench.
17. The system of claim 11, wherein the third data includes data representative of a dishing and/or erosion of the method in the at least one trench.
18. The system of claim 11, wherein the determined planarization process includes at least one of a removal rate, a polishing pressure, and chemical supplies to be used.
19. The system of claim 11, wherein the actual resistance of the metal in the at least one trench is measured and compared to the target resistance.
20. A computer-assisted system for controlling metal line resistance (RS) uniformity, in a semiconductor manufacturing process using integrated or in-line metrology, comprising:
- (A) at least one first component, to collect first data representative of at least one measurement of a first thickness of at least one dielectric deposition layer, subsequent to a chemical vapor deposition process on at least one semiconductor product;
 - (B) at least one second component, to collect second data representative of a plurality of measurements characterizing a profile of at least one trench in the at least one dielectric deposition layer, including at least depth, top critical dimension, bottom critical dimension, and at least one critical dimension along a side wall, of the at least one trench, subsequent to an etch process on the at least one semiconductor product;
 - (C) at least one third component, to collect third data representative of at least one measurement of a second thickness of the at least one dielectric deposition layer, a thickness of a metal deposited in the at least one trench, and a dishing and/or erosion of the metal in the at least one trench, on the at least one semiconductor product;
 - (D) at least one controller, to determine an area of a cross section of metal in the at least one trench at the profile and to compare the resistance of the area to a target resistance; and to determine at least one of a removal rate, polishing pressure, and chemical supplies to use in

the chemical mechanical planarization process, to leave an amount of metal in the at least one trench, approximating the target resistance in the at least one semiconductor product;

(E) wherein the at least one controller utilizes the at least one of the determined removal rate, polishing pressure, and chemical supplies in the chemical mechanical planarization process for at least one of: the at least one semiconductor product, another semiconductor product subsequent to the at least one semiconductor product, a lot of semiconductor products including the at least one semiconductor product, and a lot of semiconductor products including the other semiconductor product;

(F) wherein the deposition process, responsive to the first data, adjusts the deposition process; a lithograph process and/or the etch process, responsive to the second data, adjusts the lithography process and/or the etch process; and the planarization process, responsive to the third data, adjusts the planarization process; and

(G) wherein the at least one controller determines a variation in resistance over the plurality of semiconductor products including the at least one semiconductor product.

21. A computer program for controlling metal line resistance (RS) uniformity, in a semiconductor manufacturing process using integrated or in-line metrology, the computer program having instructions stored on at least one computer-readable medium, comprising:

(A) instructions for collecting first data representative of at least one measurement of a first thickness of at least one deposition layer, subsequent to a deposition process on at least one semiconductor product;

(B) instructions for collecting second data representative of a plurality of measurements characterizing a profile of at least one trench in the at least one deposition layer, subsequent to an etch process on the at least one semiconductor product;

(C) instructions for collecting third data representative of at least one measurement of a second thickness of the at least one deposition layer, and a thickness of a metal deposited in the at least one trench, on the at least one semiconductor product;

(D) instructions, on the computer-readable medium, for determining an area of a cross section of metal in the at least one trench at the profile and for comparing the resistance of the area to a target resistance; and

(E) instructions for determining a planarization process, so as to leave an amount of metal in the at least one trench, approximating the target resistance in the at least one semiconductor product.

22. The computer program of claim 21, further comprising instructions for utilizing the determined planarization process for at least one of: the at least one semiconductor product, another semiconductor product subsequent to the at least one semiconductor product, a lot of semiconductor products including the at least one semiconductor product, and a lot of semiconductor products including the other semiconductor product.

23. The computer program of claim 21, further comprising instructions for utilizing at least one of: the first data to adjust the deposition process, the second data to adjust a lithography process and/or the etch process, and the third data to adjust the planarization process, for the other semiconductor product subsequent to the at least one semiconductor product.

24. The computer program of claim 21, further comprising instructions for determining a variation in resistance over a plurality of semiconductor products including the at least one semiconductor product.

25. The computer program of claim 21, wherein the at least one deposition layer includes a dielectric deposition layer, and wherein the deposition process is a chemical vapor deposition process.

26. The computer program of claim 21, wherein the plurality of measurements characterizing the profile include at least depth, top critical dimension, bottom critical dimension, and at least one critical dimension along a side wall of the at least one trench.

27. The computer program of claim 21, wherein the third data includes data representative of a dishing and/or erosion of the method in the at least one trench.

28. The computer program of claim 21, wherein the determined planarization process includes at least one of a removal rate, a polishing pressure, and chemical supplies to be used.

29. The computer program of claim 21, further comprising instructions for measuring the actual resistance of metal in the at least one trench, and comparing the actual resistance to the target resistance.

30. A computer program for controlling metal line resistance (RS) uniformity, in a semiconductor manufacturing process using integrated or in-line metrology, the computer program stored on at least one computer-readable medium, comprising:

(A) instructions for collecting first data representative of at least one measurement of a first thickness of at least one dielectric deposition layer, subsequent to a chemical vapor deposition process on at least one semiconductor product;

(B) instructions for collecting second data representative of a plurality of measurements characterizing a profile of at least one trench in the at least one dielectric deposition layer, including at least depth, top critical dimension, bottom critical dimension, and at least one critical dimension along a side wall, of the at least one trench, subsequent to an etch process on the at least one semiconductor product;

(C) instructions for collecting third data representative of at least one measurement of a second thickness of the at least one dielectric deposition layer, a thickness of a metal deposited in the at least one trench, and a dishing and/or erosion of the metal in the at least one trench, on the at least one semiconductor product;

(D) instructions for determining an area of a cross section of metal in the at least one trench at the profile and for comparing the resistance of the area to a target resistance;

(E) instructions for determining at least one of a removal rate, polishing pressure, and chemical supplies to use in the chemical mechanical planarization process, to leave an amount of metal in the at least one trench, approximating the target resistance in the at least one semiconductor product;

(F) instructions for utilizing the at least one of the determined removal rate, polishing pressure, and chemical supplies in the chemical mechanical planarization process for at least one of: the at least one semiconductor product, another semiconductor product subsequent to the at least one semiconductor product, a lot of semiconductor products including the at least one semiconductor product, and a lot of semiconductor products including the other semiconductor product;

(G) instructions for utilizing at least one of: the first data to adjust the CVD process, the second data to adjust the litho and etch process, and the third data to adjust the CMP process, for the other semiconductor product subsequent to the at least one semiconductor product; and

(H) instructions for determining a variation in resistance over the plurality of semiconductor products including the at least one semiconductor product.